Notice of Allowability	Application No. 09/901,918	Applicant(s) KEN FERNALD	
	Examiner Tuan V. Thai	Art Unit 2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *amendment filed 11/24/2006 and Examiner Interview conducted on 02/02/2007*.

2. ☒ The allowed claim(s) is/are *1-3, 6-10 and 13-16 renumbered as 1-5, 7-11, 6 and 12*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☒ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

/Tuan Van/
TUAN V. THAI
PRIMARY EXAMINER

Attorney's Docket No.: CYGL-24,692

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Robert D. Norman **Group:** 2186
Serial No.: 09/901,918 **Examiner:** Tuan Thai
For: **METHOD AND APPARATUS FOR PROTECTING INTERNAL MEMORY FROM EXTERNAL ACCESS.**

EXAMINER'S AMENDMENT

1. An Examiner's Amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 C.F.R. 1.312. To ensure consideration of such an amendment, it **MUST** be submitted no later than the payment of the Issue Fee.

2. Authorization for this Examiner's Amendment was given in a telephone interview with Mr. Gregory M. Howison; Reg. No. 30,646 on February 02, 2007

3. The application has been amended as follows:

In the claims:

a. Cancel claims 4-5, 11-12 and one of the identical claims 15.

b. Please amend claims 1, 6, 8, 13 and 14 as follows:

Claim 1. (Twice Amended) A method for protecting a memory space from external access, the memory space having a plurality of logical portions, comprising the steps of:

storing in a location in the memory space on one of the logical portions thereof a plurality of lock bits, each of the lock bits associated with a separate one of the logical portions of the memory space, including the logical portions in which the lock bits are stored, and determinative as to the access thereof for a predetermined memory access operation thereon, there being at least two different memory access operations;

detecting a request for access to a desired location in one of the logical portions in the memory space for operating thereon;

comparing the requested predetermined memory access operation with the one of the lock bits associated with the one of the logical portions to which the request for access is directed and determining if access is allowed thereto for the requested predetermined memory access operation of the at least two different memory access operations; and

if allowed, performing the requested predetermined memory access operation of the at least two different memory access operations on the desired location in the memory space[.]; wherein the predetermined memory access operation includes

an erase of the associated logical portion for an addressable location therein, and wherein location the plurality of lock bits comprises storing in a variable location in the memory space the plurality of lock bits and storing the location of the lock bits in a known location in the memory space, such that in the step of comparing, the location of the lock bits is first read from the known location in the memory space and then this read location is utilized to read the lock bits from the memory space.

Claim 6. (Amended) The method of Claim [5] 1, wherein the predetermined memory access operation is an erase of the lock bits.

Claim 8. (Twice Amended) A method for protecting a memory space from an external access, the memory having a plurality of logical portions, comprising the steps of:

storing in a location in the memory space on one of the logical portions thereof a plurality of lock bits, each of the lock bits associated with a separate one of the logical portions of the memory space, including the logical portion in which the lock bits are stored, and determinative as to the access thereof for a predetermined memory access operation thereon;

detecting a request for access to a desired location in one of the logical portions in the memory space for operating

thereon;

comparing the requested predetermined memory access operation [with the] with the one of the lock bits associated with the one of the logical portions to which the request for access is directed and determining if access is allowed thereto for the requested predetermined memory access operation; and

if allowed, performing the requested predetermined memory access operation on the desired location in the memory space[.];

wherein the predetermined memory access operation includes an erase of the associated logical portion for an addressable location therein; and wherein the step of storing in a location the plurality of lock bits comprises storing in a variable location in the memory space the plurality of lock bits and storing the location of the lock bits in a known location in the memory space, such that in the step of comparing, the location of the lock bits is first read from the known location in the memory space and then this read location is utilized to read the lock bits from the memory space.

Claim 13. (Amended) The method of claim [5] 8, wherein the predetermined memory access operation is an erase of the lock bits.

Claim 14. (Amended) The method of Claim [6] 13, wherein the

predetermined memory access operation of erasing the lock bits requires that each of the lower logical portions of the memory space relative to the variable location having a relatively lower logical memory address and not containing lock bits be erased before a top most portion of memory space having a relatively higher logical address than the lower logical portions is erased, which top most portion of the memory space contains the lock bits.

Claim 15. *Noting that there are two identical claims 15 in the amendment, page 5 of 30.* ***Cancel*** *the first claim 15 (lines 4-5).*

REASONS FOR ALLOWANCE

4. The following is an Examiner's Statement of Reasons for Allowance:

The prior arts of record do not teach nor suggest, *either alone or in combination*, **all** the limitations of the claimed invention (claims 1 and 8), particularly method for protecting a memory space from the external access as being claimed in the amended claims 1 and 8 of the current invention. The prior arts of record do not teach the comparing of the requested predetermined memory access operation with the lock bits associated with one of the logical portions to determined if memory access is allowed *wherein the predetermined memory access*

operation includes an erase of the associated logical portion for an addressable location, and storing in a variable location in the memory space the plurality of lock bits and storing the location of the lock bits in a known location in the memory space such that the location of the lock bits is first read from the known location in the memory space, and the read location is utilized to read the lock bits from the memory space.

In light of the foregoing claims 1 and 8 of the present application are found to be patentable over the prior arts.

Claims 2-3, 6-7, 15, 9-10, 13-14 and 16 further limit the allowable independent claims. These claims are therefore allowable for the same reason as set forth above.

Any comments considered necessary by Applicant must be submitted no later than the payment of the Issue Fee and, to avoid processing delays, should preferably **accompany** the Issue Fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuan V. Thai whose telephone number is (571)-272-4187. The examiner can normally be reached on from 6:30 A.M. to 4:00 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mathew M. Kim can be

reached on (571)-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TVT/February 02, 2007

Tuan V. Thai
PRIMARY EXAMINER
Group 2100